Key to Tutorial 2
Counters

Exercise 1

1. For the circuit shown in Figure 1, complete the timing diagram below.

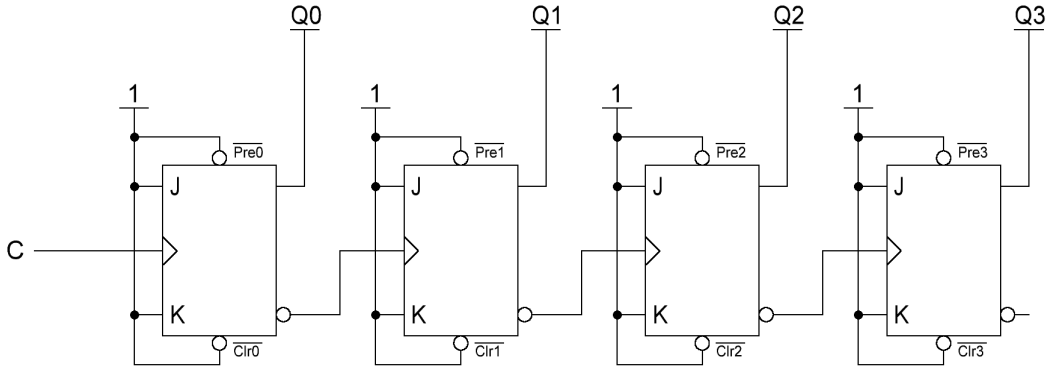
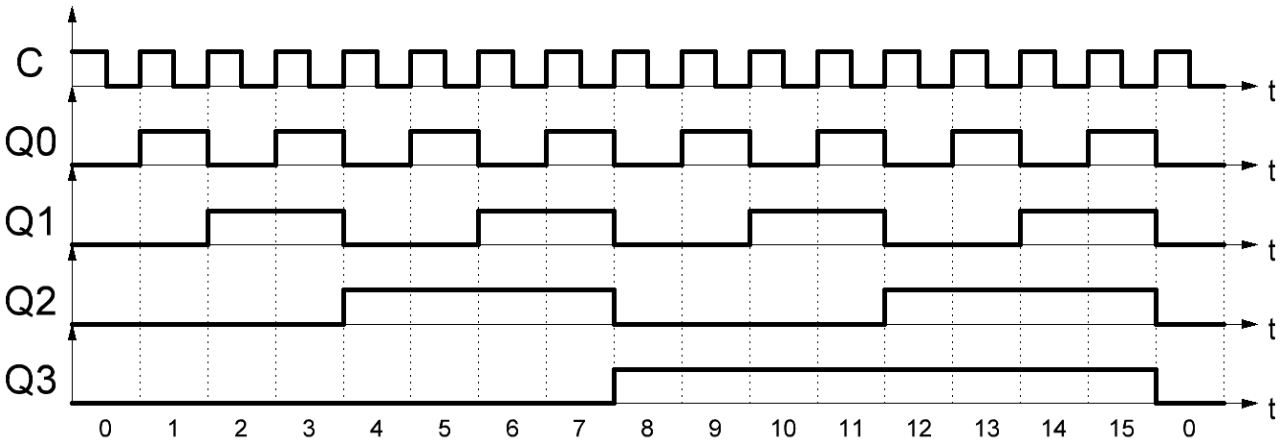


Figure 1



The JK flip-flops are positive-edge-triggered. Since $J = K = 1$, they toggle on each rising edge of their clocks:

- The output *Q0* toggles on each rising edge of *C*.
- The output *Q1* toggles on each rising edge of $\overline{Q0}$ (that is to say, on each **falling edge** of *Q0*).
- The output *Q2* toggles on each rising edge of $\overline{Q1}$ (that is to say, on each **falling edge** of *Q1*).
- The output *Q3* toggles on each rising edge of $\overline{Q2}$ (that is to say, on each **falling edge** of *Q2*).

2. What does the circuit shown in Figure 1 do?

   The 4-bit output of the circuit increases by 1 on each rising edge of *C*. This circuit is a **modulo-16 asynchronous up counter**. It counts from 0 to 15.

3. Slight changes are made to the circuit shown in Figure 1 in order to obtain the circuit shown in Figure 2. What does this new circuit do? Explain your line of reasoning.

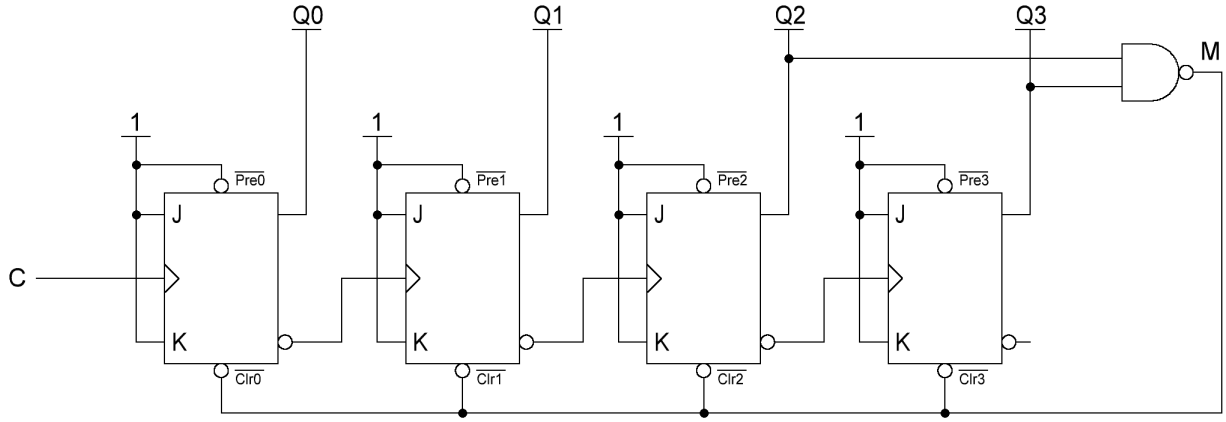


Figure 2

The purpose of the NAND gate is to detect the value 12 and force the value 0.

Let us call the output of the NAND gate *M*. As you know, the output of a NAND gate is set to 0 when both of its inputs are 1. Therefore, *M* will be set to 0 when *Q2* and *Q3* are 1 at the same time. When *M* is set to 0, all the flip-flops are reset to 0. In other words, the 4-bit output of the counter is set to 0.

When the up counter reaches 12, *Q2* = *Q3* = 1. Therefore, *M* is set to 0 and the reset inputs become active. The counter is instantly reset to 0. Then, *M* goes back to 1, the reset inputs become inactive and the counter resumes counting.

Q	Q3	Q2	Q1	Q0	M	
0	0	0	0	0	1	
1	0	0	0	1	1	
2	0	0	1	0	1	
⋮	⋮	⋮	⋮	⋮	⋮	
10	1	0	1	0	1	
11	1	0	1	1	1	
~~**12**~~	**1**	**1**	0	0	**0**	← Both *Q2* and *Q3* are 1: the reset inputs are active.
0	0	0	0	0	1	← The value 12 is instantly replaced by the value 0.
1	0	0	0	1	1	

The value 12 exists momentarily and will be long enough to reset all the flip-flops to 0. In practice, the reset pulse lasts a few nanoseconds and is related to the performance of the components.

The value 12 is detected and replaced by the value 0. This circuit is a **modulo-12 asynchronous up counter**. It counts from 0 to 11.

4. For the circuit shown in Figure 3, complete the timing diagram below.

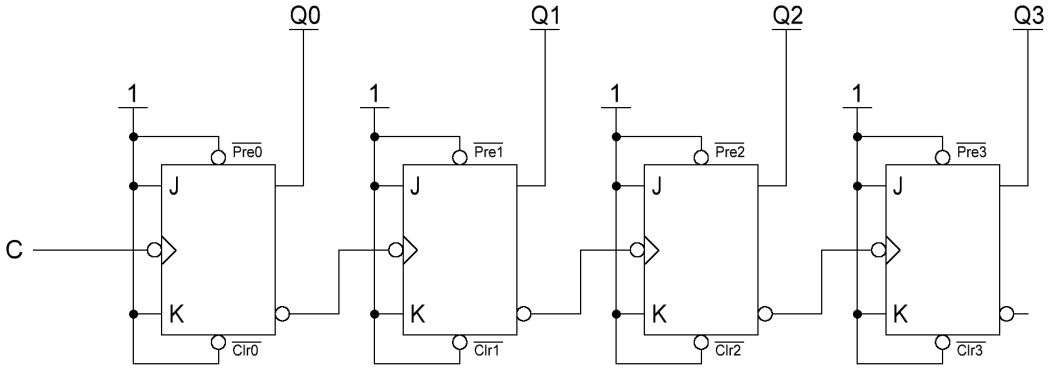
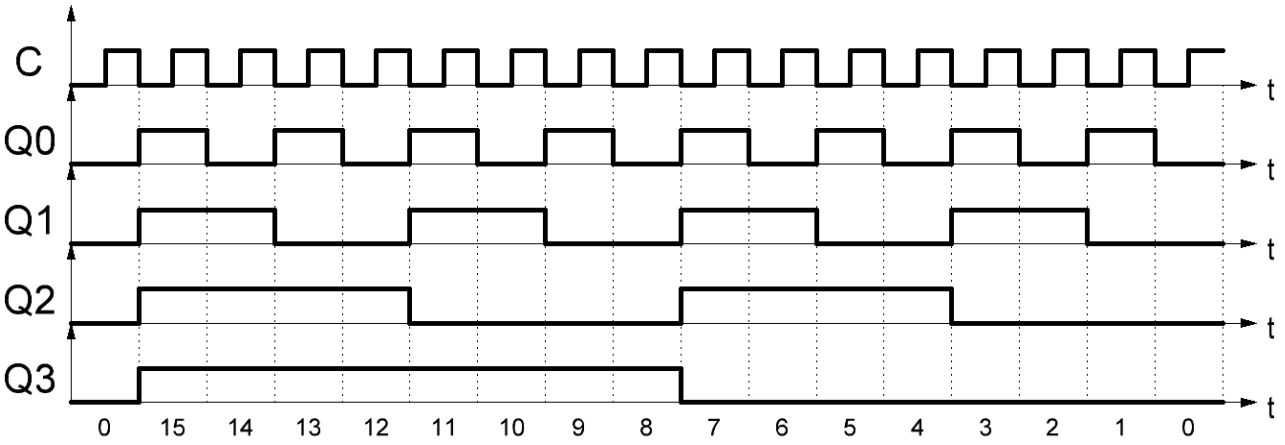


Figure 3



The JK flip-flops are negative-edge-triggered. Since $J = K = 1$, they toggle on each falling edge of their clocks:

- The *Q0* output toggles on each falling edge of *C*.
- The *Q1* output toggles on each falling edge of $\overline{Q0}$ (that is to say, on each **rising edge** of *Q0*).
- The *Q2* output toggles on each falling edge of $\overline{Q1}$ (that is to say, on each **rising edge** of *Q1*).
- The *Q3* output toggles on each falling edge of $\overline{Q2}$ (that is to say, on each **rising edge** of *Q2*).

5. What does the circuit shown in Figure 3 do?

The 4-bit output of the circuit decreases by 1 on each falling edge of *C*. This circuit is a **modulo-16 asynchronous down counter**. It counts backwards from 15 to 0.

6. Slight changes are made to the circuit shown in Figure 3 in order to obtain the circuit shown in Figure 4. What does this new circuit do? Explain your line of reasoning.

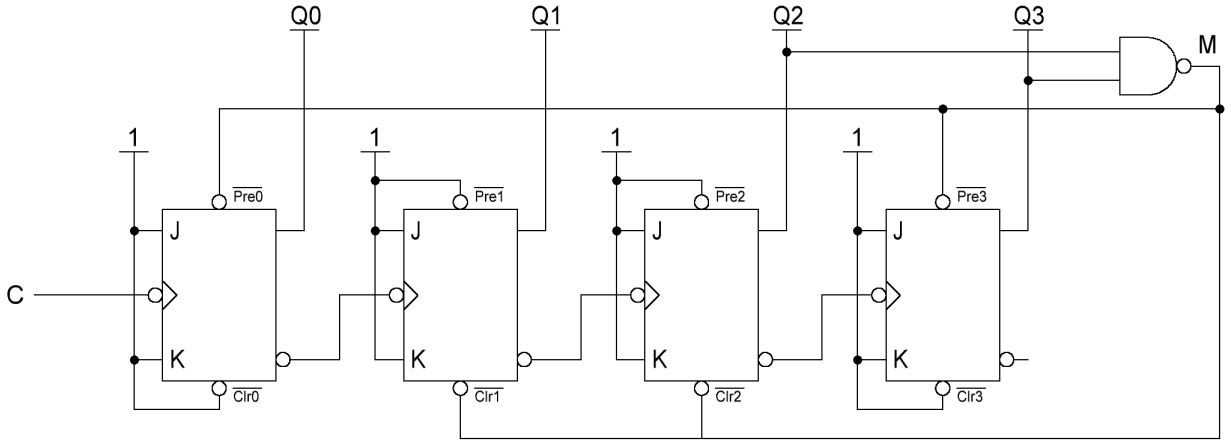


Figure 4

The purpose of the NAND gate is to detect the value 15 and force the value 9.

Let us call the output of the NAND gate *M*. As you know, the output of a NAND gate is set to 0 when both of its inputs are 1. Therefore, *M* will be set to 0 when *Q2* and *Q3* are 1 at the same time. When *M* is set to 0, *Q1* and *Q2* are reset to 0 and *Q0* and *Q3* are set to 1. In other words, the 4-bit output of the counter is set to 9 ($9_{10} = 1001_2$).

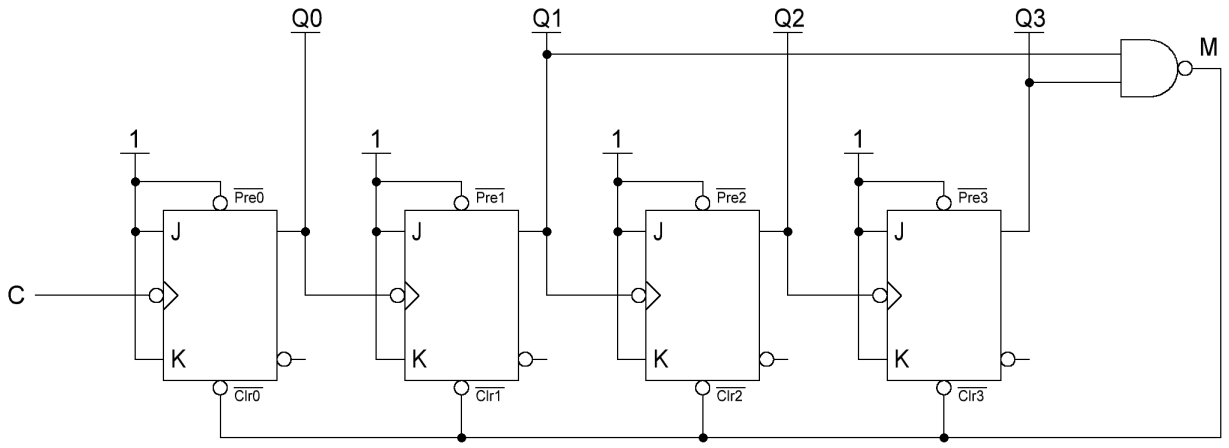
When the down counter reaches 15, *Q2* = *Q3* = 1. Therefore, *M* is set to 0 and the counter is instantly set to 9. Then, *M* goes back to 1, the set and reset inputs become inactive and the down counter resumes counting.

Q	Q3	Q2	Q1	Q0	M	
⋮	⋮	⋮	⋮	⋮	⋮	
3	0	0	1	1	1	
2	0	0	1	0	1	
1	0	0	0	1	1	
0	0	0	0	0	1	
~~**15**~~	**1**	**1**	1	1	**0**	← Both *Q2* and *Q3* are 1: the $\overline{S3}$, $\overline{R2}$, $\overline{R1}$ and $\overline{S0}$ inputs are active.
9	1	0	0	1	1	← The value 15 is instantly replaced by the value 9.
8	1	0	0	0	1	
7	0	1	1	1	1	

The value 15 exists momentarily and will be long enough to set the 4-bit output to 9. In practice, the set and reset pulses last a few nanoseconds and are related to the performance of the components.

The value 15 is detected and replaced by the value 9. This circuit is a **modulo-10 asynchronous down counter**. It counts backwards from 9 to 0.

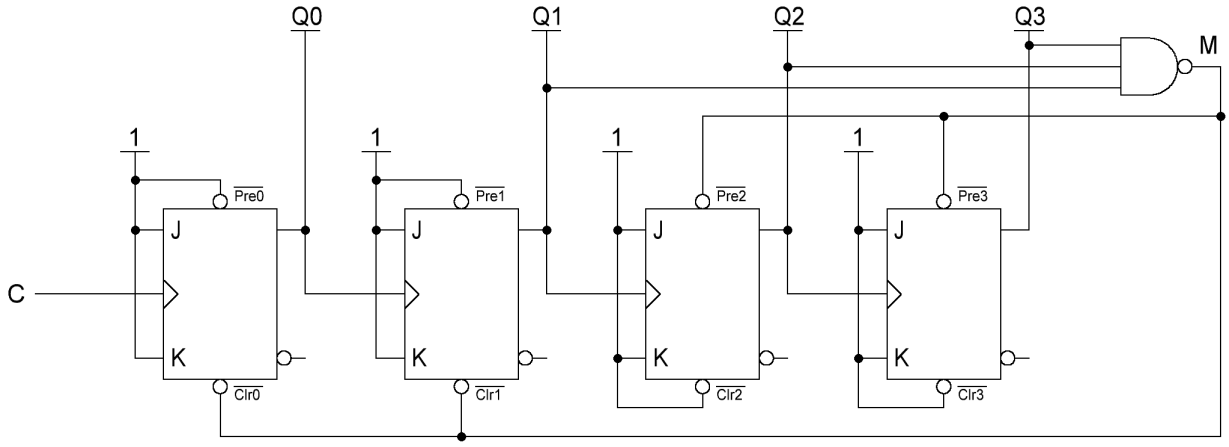
7. Wire the following flip-flops in order to design a modulo-10 asynchronous up counter.



A modulo-10 up counter counts forwards from 0 to 9.

- To count forwards, the JK inputs must be 1 so that the flip-flops toggle on each rising edge of their clocks. Then, the non-complementary output of each flip-flop must be connected to the clock input of the next flip-flop on its right. Therefore, a flip-flop will toggle on the falling edge of the previous output on its left.
- To set the modulo to 10, **the value 10 must be detected and replaced by the value 0**.
- When the 4-bit output is 10, both *Q1* and *Q3* are 1 (between 0 and 9, these two outputs are never 1 at the same time). Therefore, the *M* output of the NAND gate is set to 0 when the counter reaches 10.
- To replace the value 10 by the value 0, all the flip-flops must be reset to 0 when the counter reaches 10; that is to say, when *M* is 0.

8. Wire the following flip-flops in order to design a modulo-13 asynchronous down counter.



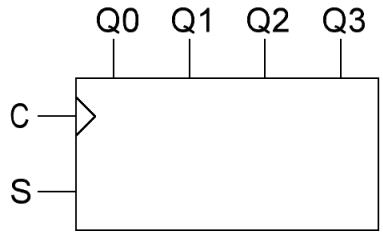
A modulo-13 down counter counts backwards from 12 to 0.

- To count backwards, the JK inputs must be 1 so that the flip-flops toggle on each rising edge of their clocks. Then, the non-complementary output of each flip-flop must be connected to the clock input of the next flip-flop on its right. Therefore, a flip-flop will toggle on the falling edge of the previous output on its left.
- To set the modulo to 13, **the value 15 must be detected and replaced by the value 12**.
- When the 4-bit output is 15, *Q1*, *Q2* and *Q3* are 1 (between 0 and 12, these three outputs are never 1 at the same time). Therefore, the *M* output of the NAND gate is set to 0 when the down counter reaches 15.
- To replace the value 15 by the value 12 ($12_{10} = 1100_2$), we have to set $Q3 = Q2 = 1$ and $Q1 = Q0 = 0$ when the down counter reaches 15; that is to say, when $M = 0$.

Exercise 2

We want to design a modulo-16 up/down counter. That is to say, a circuit that has two different modes: an up-count mode and a down-count mode. The mode can be set with an *S* input:

- S = 0 → up-count mode.
- S = 1 → down-count mode.



Draw the circuit diagram of the modulo-16 up/down counter. Use only positive-edge-triggered JK flip-flops and logic gates.

The difference between an up counter and a down counter is the connection between the output of a flip-flop and the clock input of the next flip-flop. Since our flip-flops are positive-edge-triggered, connecting the complemented outputs ($\overline{Q}$) to the next clock inputs generates an up counter; and connecting the un-complemented outputs (Q) to the same clock inputs generates a down counter. Therefore, in order to switch between the up-count mode and the down-count mode, we just have to invert the outputs that are connected to the next clock inputs according to the value of *S*. To do so, an EXCLUSIVE NOR gate can be used.

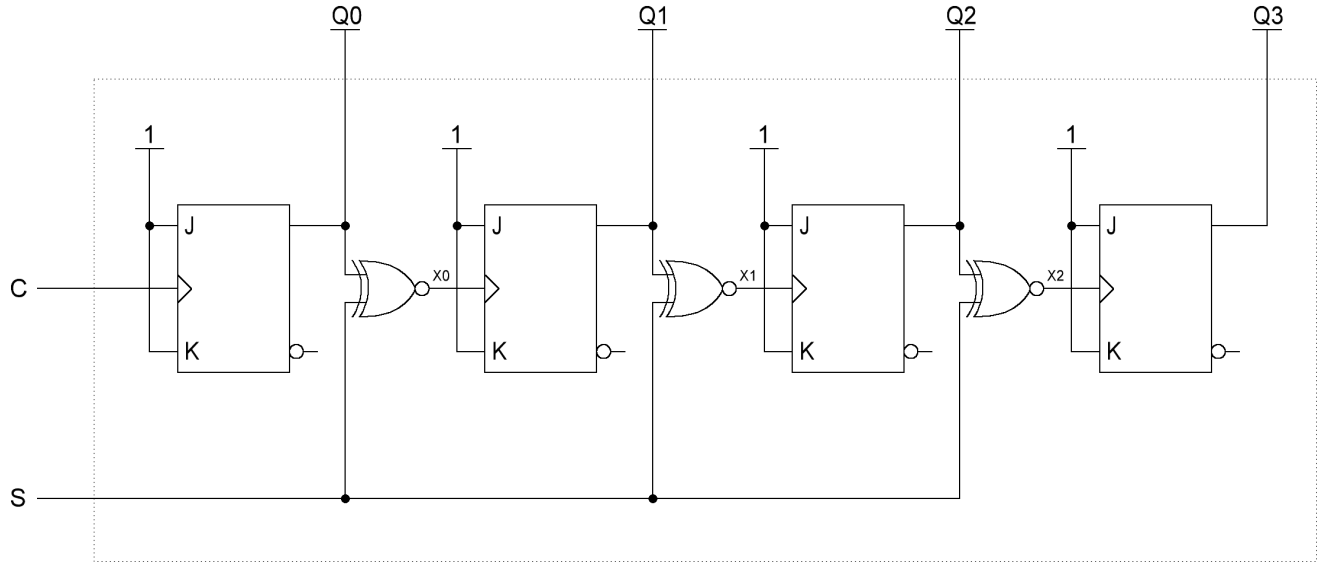
As you know, the truth table of an EXCLUSIVE NOR gate is as follows:

$$\mathbf{X = \overline{S \oplus Q}}$$

S	Q	X	
0	0	1	If $S = 0$, then $X = \overline{Q}$
0	1	0	
1	0	0	If $S = 1$, then $X = Q$
1	1	1	

- When the S input is 0, the $\overline{Q}$ outputs are connected to the next clock inputs: the circuit acts as an up counter.

- When the S input is 1, The Q outputs are connected to the next clock inputs: the circuit acts as a down counter.



Exercise 3

To begin with, you must design a modulo-7 synchronous counter using positive-edge-triggered JK flip-flops.

1. Using the excitation table of a JK flip-flop, complete the table below.

	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	Φ	0	Φ	1	Φ
1	0	0	1	0	Φ	1	Φ	Φ	1
2	0	1	0	0	Φ	Φ	0	1	Φ
3	0	1	1	1	Φ	Φ	1	Φ	1
4	1	0	0	Φ	0	0	Φ	1	Φ
5	1	0	1	Φ	0	1	Φ	Φ	1
6	1	1	0	Φ	1	Φ	1	0	Φ

According to the excitation table of a JK flip-flop, when Q0 rises from 0 to 1, J0 is 1 and K0 is either 0 or 1.

2. Obtain the most simplified expressions for *J0*, *K0*, *J1*, *K1*, *J2* and *K2*.

   These expressions can be determined from the previous table:

   - in an obvious way:
     - **K0 = 1**
     - **J1 = Q0**
     - **K2 = Q1**

   - using Karnaugh maps:

Q1 Q0

Q2 \ **J0**	**00**	**01**	**11**	**10**
0	1	Φ	Φ	1
1	1	Φ	Φ	0

J0 = $\overline{Q1}$ + $\overline{Q2}$

Q1 Q0

Q2 \ **K1**	**00**	**01**	**11**	**10**
0	Φ	Φ	1	0
1	Φ	Φ	Φ	1

K1 = Q0 + Q2

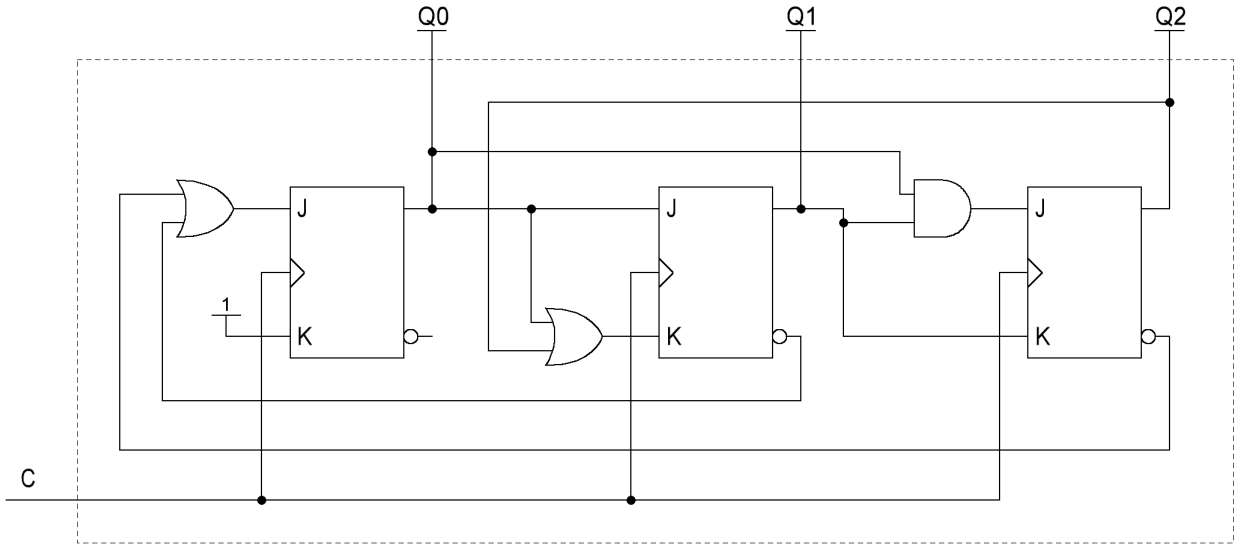
Q1 Q0

Q2 \ **J2**	**00**	**01**	**11**	**10**
0	0	0	1	0
1	Φ	Φ	Φ	Φ

J2 = Q0.Q1

3. Draw the circuit diagram of the counter.

   There is no major difficulty. You must use the expressions above to wire the flip-flops.



Then, you have to design a 3-bit synchronous Gray counter using negative-edge-triggered D flip-flops.

4. Complete the table below.

Q2	Q1	Q0	D2	D1	D0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

5. Obtain the most simplified expressions for *D0*, *D1* and *D2*.

Q2 \ Q1 Q0	**00**	**01**	**11**	**10**
0	1	1	0	0
1	0	0	1	1

D0 = $\overline{\mathbf{Q2}}.\overline{\mathbf{Q1}}$ + **Q2.Q1**

D0 = $\overline{\mathbf{Q2} \oplus \mathbf{Q1}}$

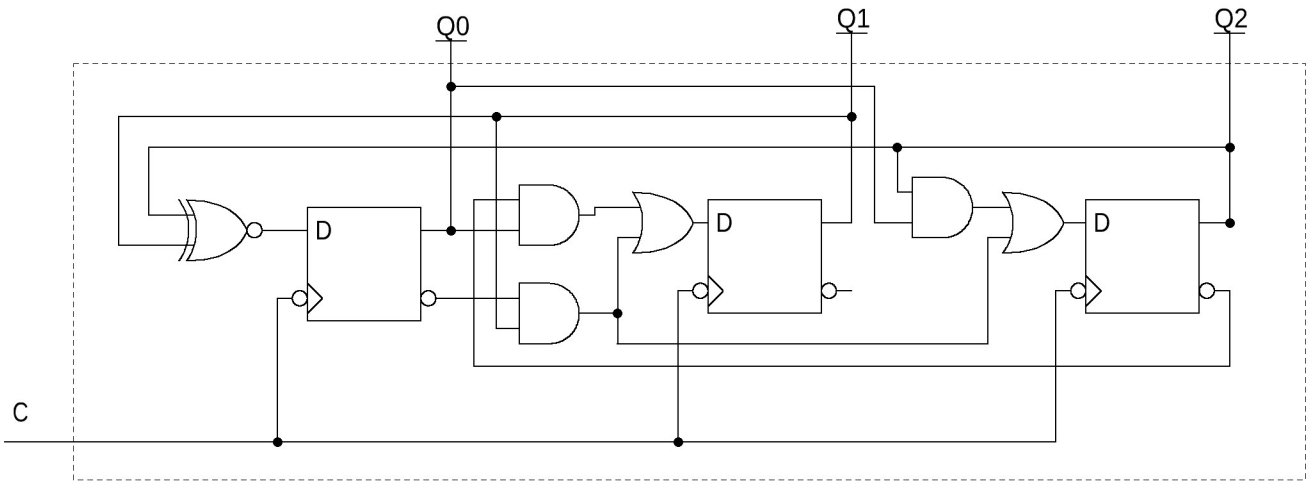
Q2 \ Q1 Q0	**00**	**01**	**11**	**10**
0	0	1	1	1
1	0	0	0	1

D1 = $\overline{\mathbf{Q2}}$**.Q0** + **Q1.**$\overline{\mathbf{Q0}}$

Q2 \ *Q1 Q0*	**00**	**01**	**11**	**10**
0	0	0	0	1
1	0	1	1	1

D2 = **Q2.Q0** + **Q1.**$\overline{\mathbf{Q0}}$

6. Draw the circuit diagram of the counter.



Lastly, you have to design the same 3-bit synchronous Gray counter but by using negative-edge-triggered JK flip-flops.

7. Complete the table below.

Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	Φ	0	Φ	1	Φ
0	0	1	0	Φ	1	Φ	Φ	0
0	1	1	0	Φ	Φ	0	Φ	1
0	1	0	1	Φ	Φ	0	0	Φ
1	1	0	Φ	0	Φ	0	1	Φ
1	1	1	Φ	0	Φ	1	Φ	0
1	0	1	Φ	0	0	Φ	Φ	1
1	0	0	Φ	1	0	Φ	0	Φ

8. Obtain the most simplified expressions for *J0*, *K0*, *J1*, *K1*, *J2* and *K2*.

J0 \ Q2 Q1 Q0	00	01	11	10
0	1	Φ	Φ	0
1	0	Φ	Φ	1

J0 = $\overline{Q1}.\overline{Q2} + Q1.Q2 = \overline{Q1 \oplus Q2}$

K0 \ Q2 Q1 Q0	00	01	11	10
0	Φ	0	1	Φ
1	Φ	1	0	Φ

K0 = $\overline{Q1}.Q2 + Q1.\overline{Q2}$ = Q1 ⊕ Q2

J1 \ Q2 Q1 Q0	00	01	11	10
0	0	1	Φ	Φ
1	0	0	Φ	Φ

J1 = Q0.$\overline{Q2}$

K1 \ Q2 Q1 Q0	00	01	11	10
0	Φ	Φ	0	0
1	Φ	Φ	1	0

K1 = Q0.Q2

J2 \ Q2 Q1 Q0	00	01	11	10
0	0	0	0	1
1	Φ	Φ	Φ	Φ

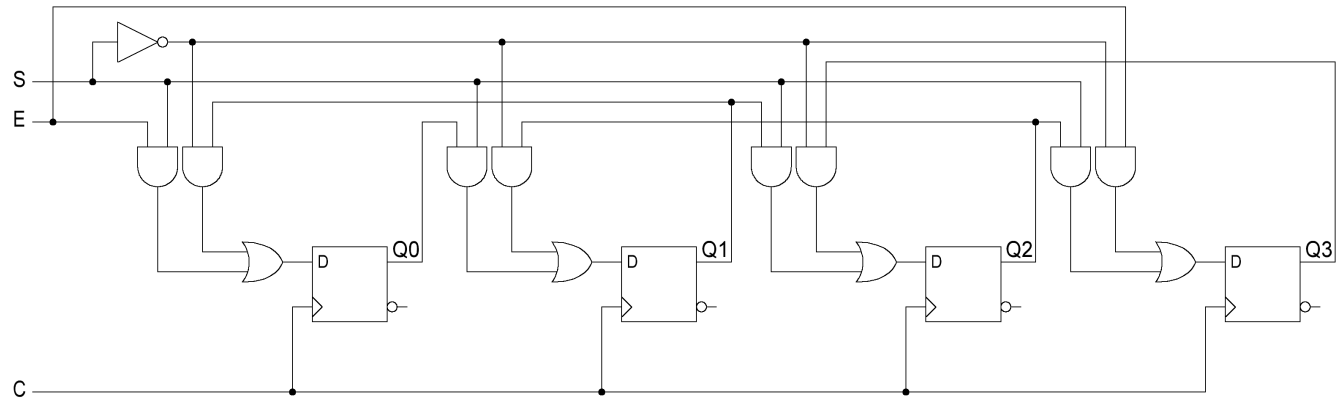
J2 = $\overline{Q0}$.Q1

K2 \ Q2 Q1 Q0	00	01	11	10
0	Φ	Φ	Φ	Φ
1	1	0	0	0

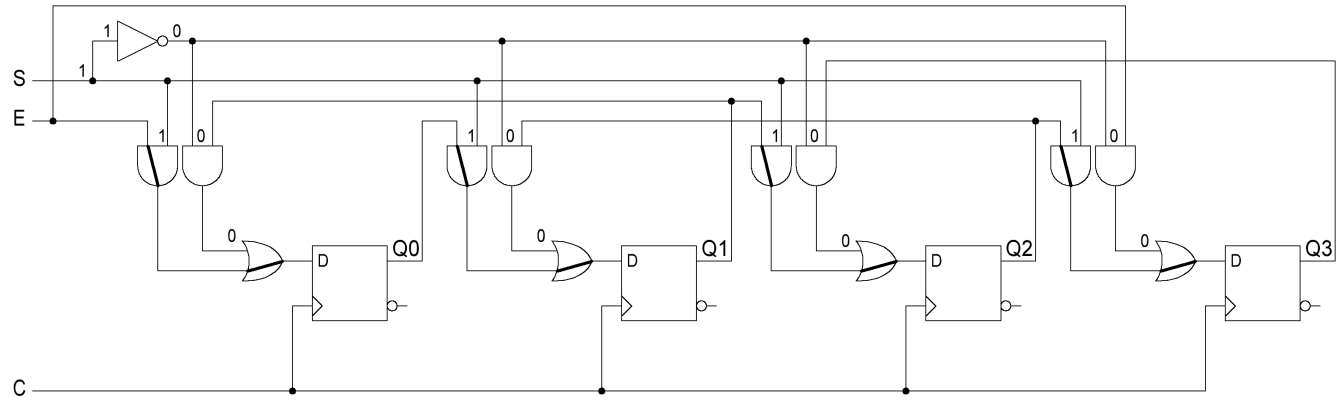
K2 = $\overline{Q0}.\overline{Q1}$

Exercise 4

Complete the timing diagram for the circuit below ($E = 0$).

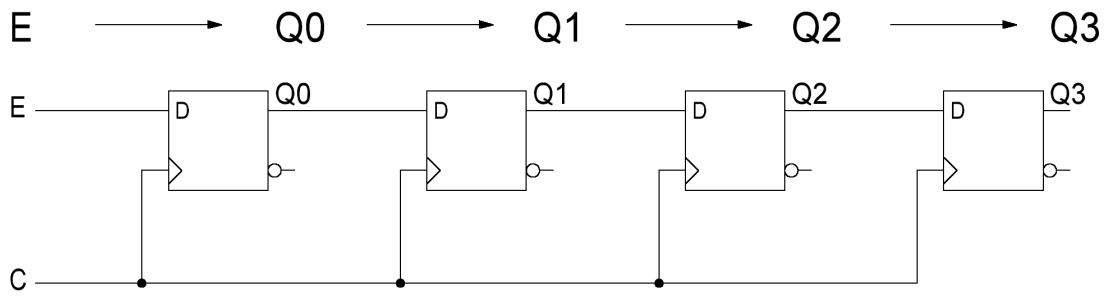


Let us investigate the circuit when $S = 1$ and find a simplified equivalent circuit.



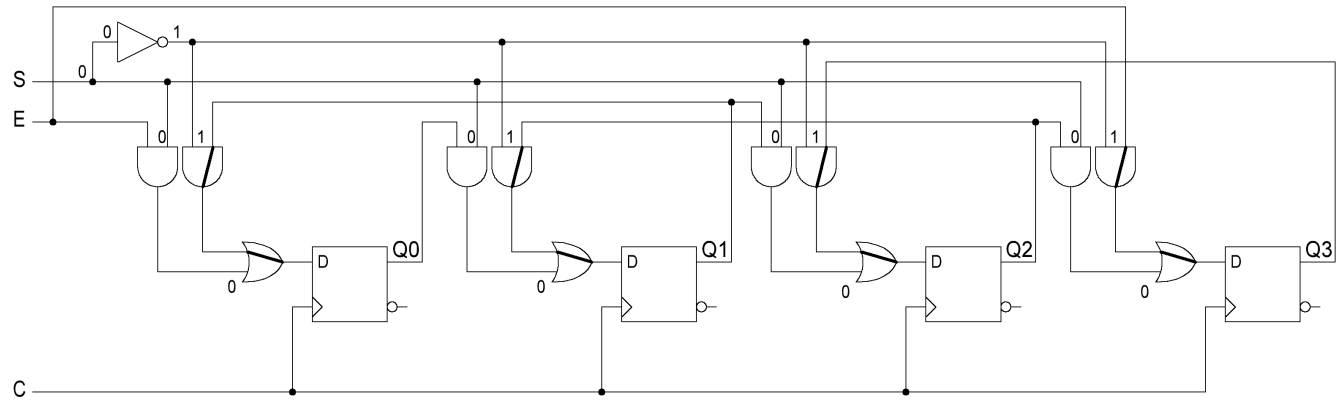
The S input is connected to some of the AND gates. Since $S = 1$, these gates can be replaced by a wire. The inverter, at the top-left of the circuit, is connected to the remaining AND gates. Since the output of the inverter is 0, the outputs of these AND gates are 0. Then, these outputs are connected to the inputs of the OR gates. Therefore, these OR gates can be replaced by a wire.

After being simplified, here is what the circuit looks like:

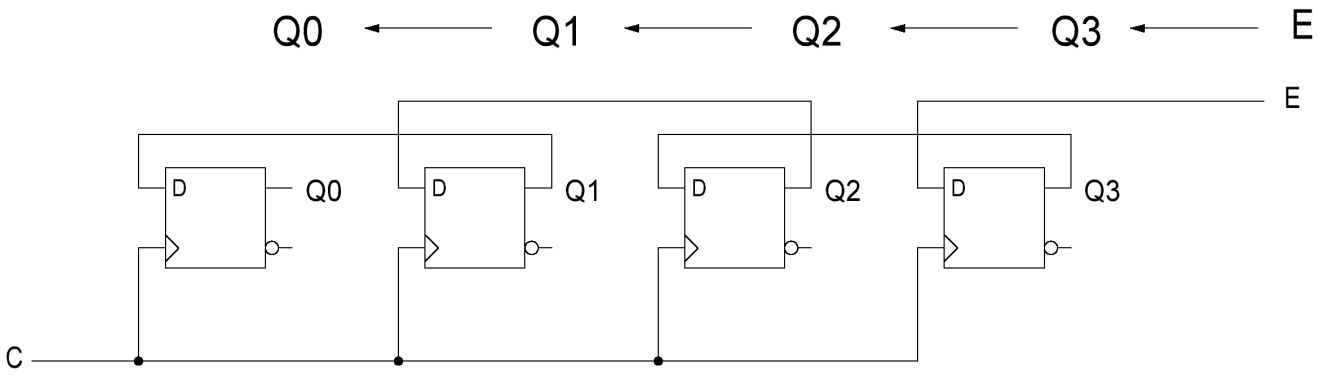


When a *D* flip-flop is triggered, the value at its *D* input is transferred to its *Q* output. Therefore, on each rising edge of *C*, each output takes on the value from the output on its left (except for the flip-flop on the far left: *Q0* takes on the value of *E*). This circuit is a four-stage shift register. Since *Q0* is the least significant bit, it is a **four-stage left-shift register**.

With the same line of reasoning, let us investigate the circuit when $S = 0$ and find a simplified equivalent circuit.



After being simplified, here is what the circuit looks like:



This simplified circuit is a **four-stage right-shift register** and Q3 takes on the value of E.

Therefore, the whole circuit is a **bi-directional four-stage shift register**. It has a control *S* input that selects the shift direction and a data *E* input that contains a new bit to be shifted.

Completing the timing diagram is easy. All you have to do is shift some bits in one direction or another.

